trench to provide a gate dielectric for capacitively coupling the gate to the channel-accommodating region,

(c) depositing and then etching back semiconductor gate material to provide a semiconductor gate part on the dielectric layer in the trench without protruding above the masking pattern at the window, and

(d) then providing at the window a thickness of metal silicide material at the top of the semiconductor gate part sufficient to form a silicide upstanding part of the gate having a top and sidewalls that protrude upward above the level of the body surface, the gate dielectric at least adjacent to the channel-accommodating region being protected from the metal silicide material by at least the semiconductor part of the gate and by the protrusion of its silicide part above the level of the body surface.

8. (Original) A method according to Claim 7, wherein the said window of the masking pattern provided in step (a) is a wide window that is narrowed to a narrower window by providing sidewall extensions at the sidewalls of the wide window, the trench is etched in step (b) at the narrower window, and the source region is provided so as to be self-aligned with the trench-gate by means of these sidewall extensions.

9. (currently amended) A method according to Claim 7 ~~or Claim 8~~, wherein, after the step (c), the following steps are carried out:

- sidewall extensions are provided at sidewalls of the window of step (a) to form a further window that is narrower than the width of the trench,
- the metal silicide material is deposited in the said further window in step (d) so as to form the silicide upstanding part of the trench-gate spaced from the walls of the trench,

- an insulating overlayer is provided over the silicide upstanding part of the trench-gate,
- and the masking pattern is then removed before providing a source electrode to contact the source region and to extend over the insulating overlayer over the trench-gate.

10. (Currently amended) A method according to Claim 7 ~~or Claim 8~~, wherein the semiconductor gate material provided in the trench in step (c) comprises polycrystalline silicon protruding above the level of the body surface, sidewalls of the protruding polycrystalline silicon are exposed, and a silicide-forming metal is then deposited on the protruding polycrystalline silicon and is alloyed into the sidewalls and top of the protruding polycrystalline silicon so as to form the silicide upstanding part on top of remaining silicon semiconductor gate material in the trench.

11. (Original) A method of manufacturing a trench-gate semiconductor device having source and drain regions which are separated by a channel-accommodating region adjacent to the trench-gate, including the following sequence of steps:

(a) providing at a surface of a semiconductor body a masking pattern comprising upper and lower layers through which a window extends at an area of the body where the trench-gate is to be provided,

(b) etching a trench for the gate into the body at the window, and forming a gate dielectric layer at the walls of the trench in the semiconductor body,

(c) providing silicon gate material in the trench and in the window, and then removing the upper layer of the masking pattern such that the silicon gate material has an upstanding upper part that protrudes above the adjacent surface of the lower layer of the masking pattern,

(d) depositing a silicide-forming metal over the silicon gate material and over the lower layer of the masking pattern, and heating at least the metal to grow a metal silicide into the silicon gate material from the top and side-walls of the upstanding upper part, and

(e) removing the un-silicided metal so as to leave a partially-silicided trench-gate protruding from the semiconductor body.

12. (Original) A method according to Claim 11, wherein the upper layer of the masking pattern is thicker, for example at least 5 times thicker, than the lower layer.

13. (Currently amended) A method according to Claim 11 ~~or Claim 12~~, wherein the upper layer of the masking pattern comprises silicon dioxide, and the lower layer comprises silicon nitride on a thinner layer of silicon dioxide on the semiconductor body surface.

14. (Currently amended) A method according to ~~any one of Claims 10 to 13~~Claim 10, wherein the deposited silicide-forming metal is heated by rapid thermal annealing to form the silicide with the silicon gate material.

15. (Currently amended) A method according to Claim 7~~any one of Claims 7 to 14~~, wherein the surface of the metal silicide upstanding part is subsequently oxidised so as to grow an insulating oxide adjacent to the silicide, which insulating oxide forms at least a part of an insulating over-layer provided over the top of the protruding part of the trench-gate, and a source electrode is deposited on the insulating over-layer and on an exposed surface area of the semiconductor body beside the trench-gate after removing the lower layer of the masking pattern.

16. (Original) A method according to Claim 15, wherein the masking pattern includes a silicon nitride layer that is used to mask the underlying body surface from oxidation during the growth of the insulating oxide adjacent to the silicide.